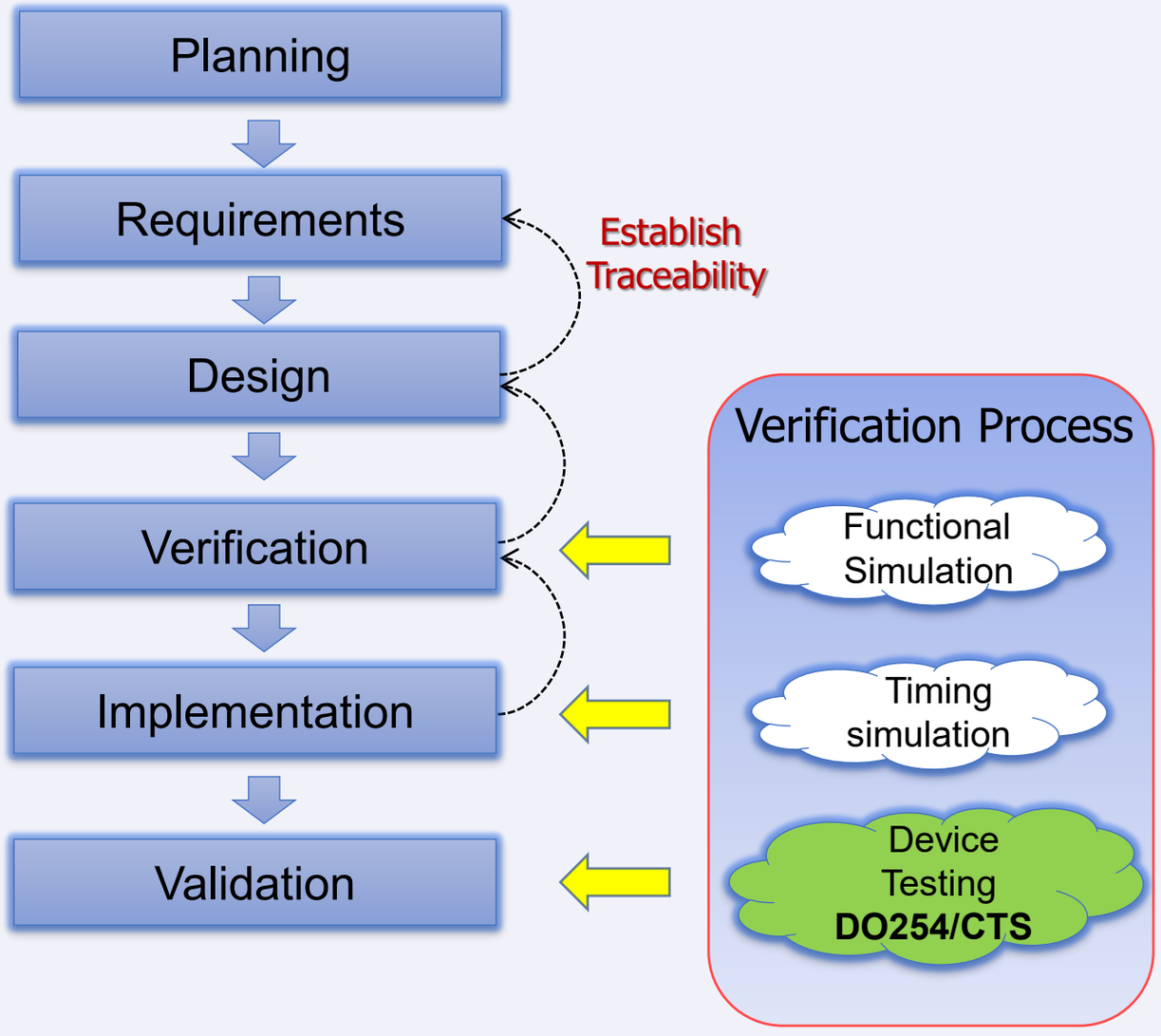
Design and Verification Services
FPGA Flow DO-254 Compliance



- **Planning Process**
  - DO-254 Training and Consulting Services
  - FPGA Design and Verification Training
  - System Verilog based UVM Verification Training
  - Establish project plans and standards
  - Define strategy for compliance
- **Requirements**
  - Management and Traceability
  - Allocate system functions to hardware
  - Create derived requirements
- **Design Process**
  - High level description of design
  - Identify major components
  - RTL design
- **Verification Process**
  - Functional Simulations
  - Timing Simulations
  - Directed Tests
  - System Verilog based UVM tests
  - Formal Verification
- **Implementation**
  - Synthesis
  - Place and Route
  - Timing Model
  - Generate bitstream file
- **Validation**
  - Verify design on DO-254/CTS boards
  - FPGA Validation

www.yongatek.com
Teknopark İstanbul Sanayi Mah. No:1/9 A Kat:3 34906
Pendik, İstanbul, TÜRKİYE Tel:+90 216 504 14 10
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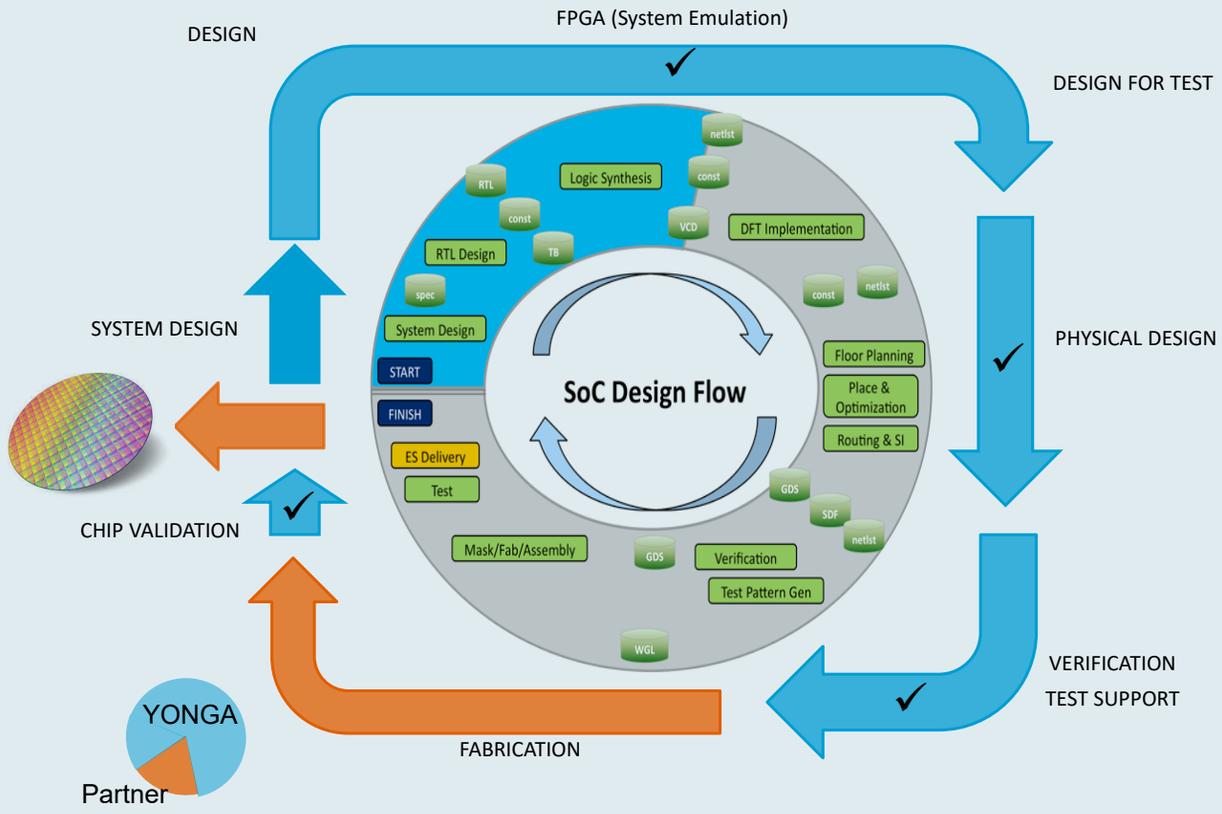
Design and Verification Services
Soc/ASIC Flow for DO-254 Compliance



YONGATEK team have big experience in ASIC design and verification flow in different CMOS technologies (from 0,35 um to 20 nm).

- System Design
  - Specification
  - System Model Development
  - Requirement Management and Traceability
- Design
  - High Level Design
  - Micro Architecture Documentation
  - RTL Coding with VHDL or Verilog
  - Functional Simulations
    - ▪Directed Tests
    - ▪System Verilog based UVM Tests
  - Formal Verification
- Logic Synthesis
  - Constraints
  - DFT (Design for Tests) Implementation
- Gate Level Simulations
  - STA for hand-off before backend
- FPGA prototyping for ASIC with big CTS boards
- Psychical Design
  - Floor Planning
  - Place and Route
  - DRC
- Verification and Test Supports
  - STA for sign-off before tape-out
  - Test Pattern Generations
- Tape-out and Fabrication
- Chip Validation
- Cost effective Supply Chain Management

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